

ABSTRACT:

A circuit comprises a first JFET (21) connected in series to a second JFET (22) wherein a gate (26) of the first JFET (21) is connected to a source of the second JFET (22) and is connected to a load (30) and is not connected to ground. The gate of the second JFET (22) is connected to ground. The JFETs are preferably formed by silicon on insulator

5 integration technology.

(Fig. 2)